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# Description

# APPARATUS AND METHOD FOR IMAGE FRAME SYNCHRONIZATION

## BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The invention relates to video display devices, and more particularly, to converting from a first display resolution to a second display resolution using image frame synchronization.

[0003] 2. Description of the Prior Art

[0004] Graphics systems display images on display screens. For example, a computer system may display an image on a flat-panel monitor. Television systems and cameras are additional examples of such graphics systems. To achieve the display of an image, the image is generally represented by image data (e.g., RGB data), and display signals are generated from the image data. The standard VGA format is 640 pixels wide by 480 pixels high.

[0005] Fig.1 shows a timing diagram 10 of the typical display signals for a VGA system. The display signals including a vertical sync signal VS indicating the beginning of each screen, also called a frame; a horizontal sync signal HS indicating the beginning of each row, also called a horizontal line; a data enable line indicating the pixel data in each scan line, and a clock signal. As shown in Fig.1, a first frame starts at the first leading edge E1 of the vertical sync signal and a second frame starts at the second leading edge E2.

[0006] As graphics systems continue to have higher and higher display resolutions, a need emerges to convert image data from a first resolution to a second resolution. Graphics systems typically use special circuitry to convert image resolution. Examples of such circuitry include the well-known graphics controller chips typically housed on a motherboard of a computer system and LCD control chip sets provided with LCD panels and video cameras.

[0007] For most new displays, it is sufficient to use the same frame rate for the source display signals and the destination display signals, simplifying the design and reducing the required memory. This technique is called frame synchronization and involves generating a destination frame

for each source frame received and outputting the destination frames at the same rate as the source frames are received.

[0008] A significant timing problem is inherent in frame synchronization. The source signals contain both visible horizontal lines and non-visible horizontal lines. Resolution is normally specified in terms of visible pixels only but, in actuality, there are the additional non-visible horizontal lines and non-visible pixels at the ends of the visible horizontal lines. If a resolution is converted from x to y then the ratio of x:y must also hold for the non visible horizontal lines. An example of where difficulties are encountered is when converting frame signals for a typical VGA system. As previously mentioned, the typical VGA system is 640x480, or 480 horizontal lines; however, in actuality there are approximately 504 horizontal sync signals sent for each vertical sync signal. The extra horizontal lines are not visible but are present to allow the display device time to return to the upper left corner before beginning the next refresh cycle. The ratio of visible source horizontal lines to visible destination horizontal lines must be equal to the ratio of total source horizontal lines to total destination horizontal lines. If a destination display device hav-

ing a resolution of 1280x1024 is to be used, this equates to 1024/480*504 or a total of 1075.2 destination horizontal lines. The value of the destination horizontal lines must be an integer but if this value is rounded up, overflow occurs because the source frame rate will be higher than the destination frame rate. Conversely, if this value is rounded down, underflow occurs because the source frame rate will be lower than the destination frame rate.

## SUMMARY OF INVENTION

[0009] It is therefore a primary objective of the claimed invention to provide an apparatus and method for image frame synchronization, to solve the above-mentioned timing problem and prevent overflow and underflow.

[0010] According to the claimed invention, an apparatus for converting a source frame signal to a destination frame signal is disclosed. The source frame signal is received at a first frame rate, and the destination frame signal is output at a second frame rate. The apparatus comprises a converter for converting the source frame signal to the destination frame signal having a destination clock signal at a destination clock frequency; and a frequency synthesizer for generating the destination clock signal and adjusting the destination clock frequency such that the first frame rate

and the second frame rate are substantially the same.

[0011] According to the claimed invention, a method of frame synchronization for converting a source frame signal to a destination frame signal is disclosed. The source frame signal is received at a first frame rate, and the destination frame signal is output at a second frame rate. The method comprises the following steps: generating the destination frame signal according to the source frame signal, wherein the destination frame signal includes a destination clock signal at a destination clock frequency; and adjusting the destination clock frequency such that the first frame rate and the second frame rate are substantially the same.

[0012] It is an advantage of the claimed invention that by adjusting the destination clock frequency and fine-tuning the vertical sync signal, the leading edge of the vertical sync signal is synchronized with the horizontal sync signal when the frame synchronization apparatus receives the input vertical sync signal and that the first frame rate and the second frame rate are substantially the same.

[0013] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the

preferred embodiment that is illustrated in the various figures and drawings.

## Brief Description of Drawings

[0014] Fig.1 is a timing diagram of typical video signals according to the prior art.

[0015] Fig.2 is a timing diagram of video signals according to the present invention.

[0016] Fig.3 is a timing diagram of the last horizontal sync signal and the vertical sync signal of Fig.2.

[0017] Fig.4 is a frame synchronization apparatus according to the present invention.

[0018] Fig.5 is a flowchart showing the method of image frame synchronization according to the present invention.

## Detailed Description

[0019] Fig.2 shows a timing diagram of destination video signals according to the present invention. Fig.2 includes the vertical sync signal VS, the horizontal sync signal HS, and the clock signal. A first frame starts with the edge E3 and contains horizontal rows indicated by the HS signal. A second frame starts with the edge E4 and also contains horizontal rows indicated by the HS signal. For simplicity of the diagram, the data enable signal and the pixel data

signals are not shown in Fig.2; however, as in Fig.1, each horizontal row also contains a data enable signal (Data_en) indicating the pixel data (Pixel_data). Because the video signals (VS, HS, Data_en, Pixel_data) are synchronous with the clock signal, decreasing or increasing the frequency of the clock signal expands or compresses the frame respectively. As shown in Fig.2, at the edge E4, the clock frequency is lowered from a first frequency $f_1$ to a second frequency $f_2$. The distance between the start of the first frame (the first frame starts at the edge E3) and the start of the second frame (edge E4) is less than the distance between the start of the second frame (edge E4) and the start of a third frame (edge E5). In other words the frame rate before edge E4 is higher than the frame rate after edge E4.

[0020] By adjusting the destination frame rate, the underflow and overflow problems of the prior art are solved. When an underflow condition occurs, the source frame rate is slightly lower than the destination frame rate. In this situation, the destination clock frequency is lowered such that the destination frame rate is equal to the source frame rate. When an overflow condition occurs, the source frame rate is slightly higher than the destination frame rate. In

this situation, the destination clock frequency is raised such that the destination frame rate is equal to the source frame rate. Furthermore, the range of acceptable clock frequencies for most digital display devices is quite wide and adjusting the frequency in this way does not disrupt-normal operations.

[0021] Fig.3 shows a timing diagram 30 of the relationship between the vertical sync signal D_VS and the horizontal sync signal D_HS. For some destination display devices, particularly some LCD panels, there is a hardware restriction limiting the time $T_{LIMIT}$ between the last horizontal sync signal D_HS and the vertical sync signal D_VS. In the conventional frame-synchronization apparatus, the vertical sync signal D_VS is locked (synchronized) with the input vertical sync signal I_VS. Thus, the time $T_{LAST\_LINE}$ is smaller than $T_{LIMIT}$ and cannot satisfy this timing requirement. For some display devices, the video signals need to comply with this restriction (the timing range $T_{LIMIT}$) or the display device will not function properly.

[0022] To satisfy this timing requirement, the frame synchronization apparatus can fine-tune the vertical sync signal D_VS such that the leading edge E7 of the vertical sync signal D_VS is synchronized with the horizontal sync sig-

nal D_HS when the frame synchronization apparatus receives the input vertical sync signal I_VS. Thus, the time $T_{LAST\_LINE}$ can satisfy the timing range $T_{LIMIT}$ of the display device. By adjusting the destination clock frequency, the frame synchronization apparatus can fine-tune the vertical sync signal D_VS and adjust the destination clock frequency to maintain the destination frame rate and satisfy the timing requirement.

[0023] Fig.4 shows a frame synchronization apparatus according to the present invention. The frame synchronization apparatus 40 includes a converter 42, a First-In-First-Out (FIFO) buffer 44, and a frequency synthesizer 46. Source video signals at a first display resolution are received at a first frame rate and stored in the FIFO 44. The FIFO 44 stores incoming pixel data until read out of the FIFO 44 by the converter 42 to convert from the first resolution to the second resolution. For each image frame in the source video signals, the converter 42 generates a destination frame in the destination video signals at a second frame rate. The converter 42 uses the clock signal generated by the frequency synthesizer 46 as the destination clock signal and all signals in the destination video signals are synchronous with the destination clock signal. Besides us-

ing the clock signal provided by the frequency synthesizer, the structure and the operation of the converter 42 are well known by people skilled in the art and further description of the detailed operation of the converter 42 is hereby omitted. It should also be noted that although a FIFO 44 is used as the buffer, this is for example only and any buffer implementation can be used.

[0024] If the first frame rate is higher than the second frame rate, pixel data will overflow the FIFO 44 and an overflow signal is sent to the frequency synthesizer 46. To increase the second frame rate, the frequency synthesizer 46 increases the destination clock frequency such that the FIFO 44 is no longer in the overflow condition. When the destination clock frequency is increased, the destination frame takes less time to transmit and the second frame rate is increased. Conversely, if the first frame rate is lower than the second frame rate, pixel data will be read out of the FIFO 44 too quickly and the FIFO 44 will underflow. In this situation, an underflow signal is sent from the FIFO 44 to the frequency synthesizer 46. To decrease the second frame rate, the frequency synthesizer 46 decreases the destination clock frequency such that the FIFO 44 is no longer in the underflow condition. The frequency synthe-

sizer 46 adjusts the destination clock frequency such that the pixel data in the FIFO 44 remains above a minimum level and below a maximum level. In this stable condition, the first frame rate and the second frame rate are substantially the same.

[0025] In the preferred embodiment of the present invention, the destination clock frequency is only adjusted once at initial startup. Once the second frame rate is adjusted to substantially the same rate as the first frame rate, no further adjustments of the clock frequency are necessary.

[0026] It should be noted that the frequency synthesizer 46 needs to adjust the destination clock frequency with an adjustment resolution sufficient to prevent overflow and underflow. As an example of how insufficient frequency synthesizer 46 resolution affects the frame synchronization apparatus 40, consider the case of overflow. If the FIFO 44 is in an overflow condition, the frequency synthesizer 46 must increase the frequency of the destination clock signal in order to increase the destination frame rate. However, if the resolution of the adjustment is insufficient, when the frequency is increased by a single unit of adjustment, the FIFO 44 will immediately enter the underflow condition because the destination frame rate be-

comes too fast. Likewise, in the underflow condition, when the frequency is decreased by a single unit of adjustment, the FIFO 44 will immediately enter the overflow condition because the destination frame rate becomes too slow. This unit of adjustment is referred to as the adjustment resolution and must be small enough to allow the second frame rate to be substantially the same as the first frame rate, eliminating both the overflow and underflow conditions of the FIFO 44.

[0027] The following formula can be used to calculate a sufficient adjustment resolution for the frequency synthesizer 46:

$$\text{Adjustment Resolution} < \frac{1}{2}\frac{(HorizontalVisible)}{HorizontalTotal \bullet VerticalTotal}$$

[0028] In the above formula, the *HorizontalVisible* parameter refers to the number of visible pixels in each horizontal line. For example in a typical SXGA system, the number of visible pixels in each horizontal line is 1280. The HorizontalTotal

parameter refers to the total number of pixel data for each horizontal line. As can be seen from Fig.1, only the pixels indicated by the data enable signal (Data_en) are visible on the screen. There are normally additional non-visible pixels, also referred to as porch signals, included in each horizontal line. For a typical SXGA system, the total number of pixel data for each horizontal line is 1344. Similarly the *VerticalTotal* parameter refers to the total number of horizontal lines in each frame. This number is normally greater than the visible lines on the display device, and for a typical SXGA system, *VerticalTotal* is also equal to 1066. Using the above formula for the SXGA example, the adjustment resolution equates to a value of less than $4.47 \times 10^{4}$ (or less than $2^{-11}$), meaning the destination clock frequency should be adjustable in increments of less than $2^{-11}$ of the original clock frequency.

[0029] Fig.5 shows a flowchart 50 illustrating the method of frame synchronization according to the present invention. The flowchart 50 comprises the following steps:

[0030] Step 52:Check whether incoming pixel data in a buffer or memory remains above a minimum level and below a maximum level. In this stable condition, the first frame rate and the second frame rate are substantially the same

so proceed to step 60, otherwise proceed to step 54.

[0031] Step 54:Check for an overflow condition. If an overflow condition exists then proceed to step 58, if not (underflow) then proceed to step 56.

[0032] Step 56:Decrease the destination clock frequency to lower the second frame rate. Proceed to step 52.

[0033] Step 58:Increase the destination clock frequency to increase the second frame rate. Proceed to step 52.

[0034] Step 60:Determine if the timing requirements for the last horizontal sync signal and the vertical sync signal of the destination display are satisfied. If satisfied then end, if timing adjustment is needed then proceed to step 62.

[0035] Step 62:Fine-tuning the vertical sync signal D_VS. The leading edge E7 of the vertical sync signal D_VS is synchronized with the horizontal sync signal D_HS when the frame synchronization apparatus receives the input vertical sync signal I_VS. Because the second frame rate must remain constant, the destination clock frequency during the next of the frame must be adjusted to ensure the second frame rate stays substantially the same as the first frame rate.

[0036] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made

while retaining the teachings of the invention. Accordingly, that above disclosure should be construed as limited only by the metes and bounds of the appended claims.